OIPE
DEC 22 2006
PATENT & TRADEMARK OFFICE

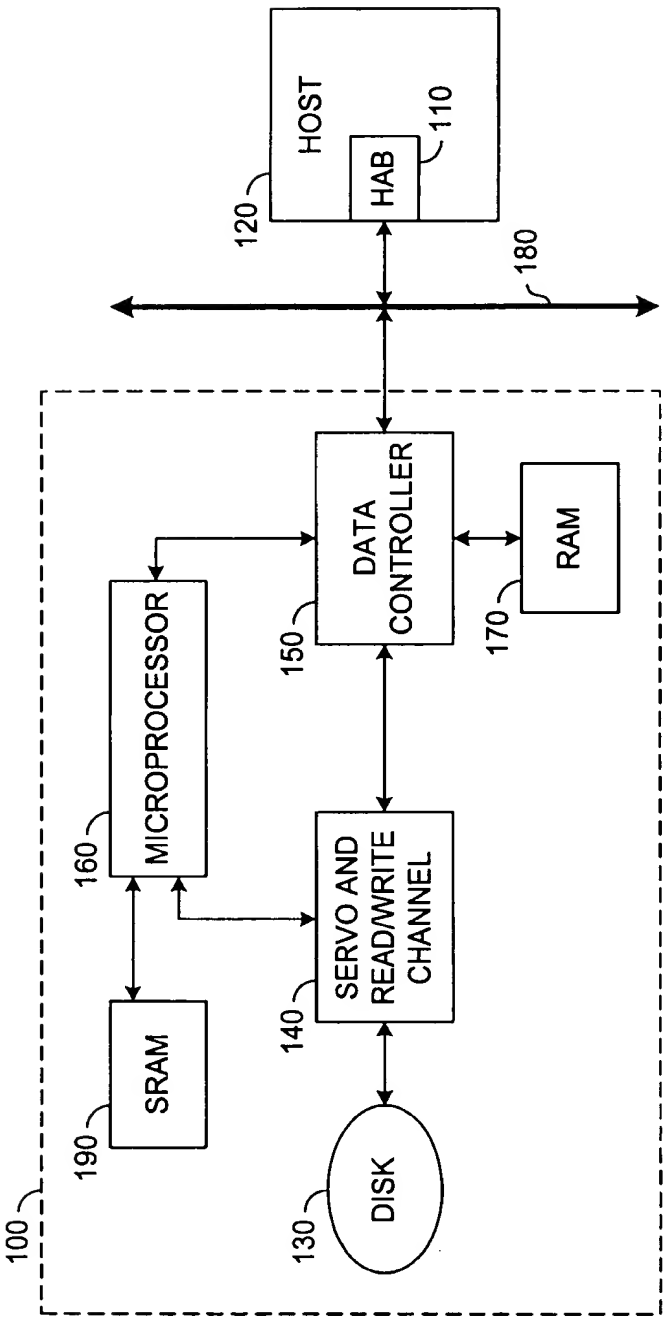


FIG. 1

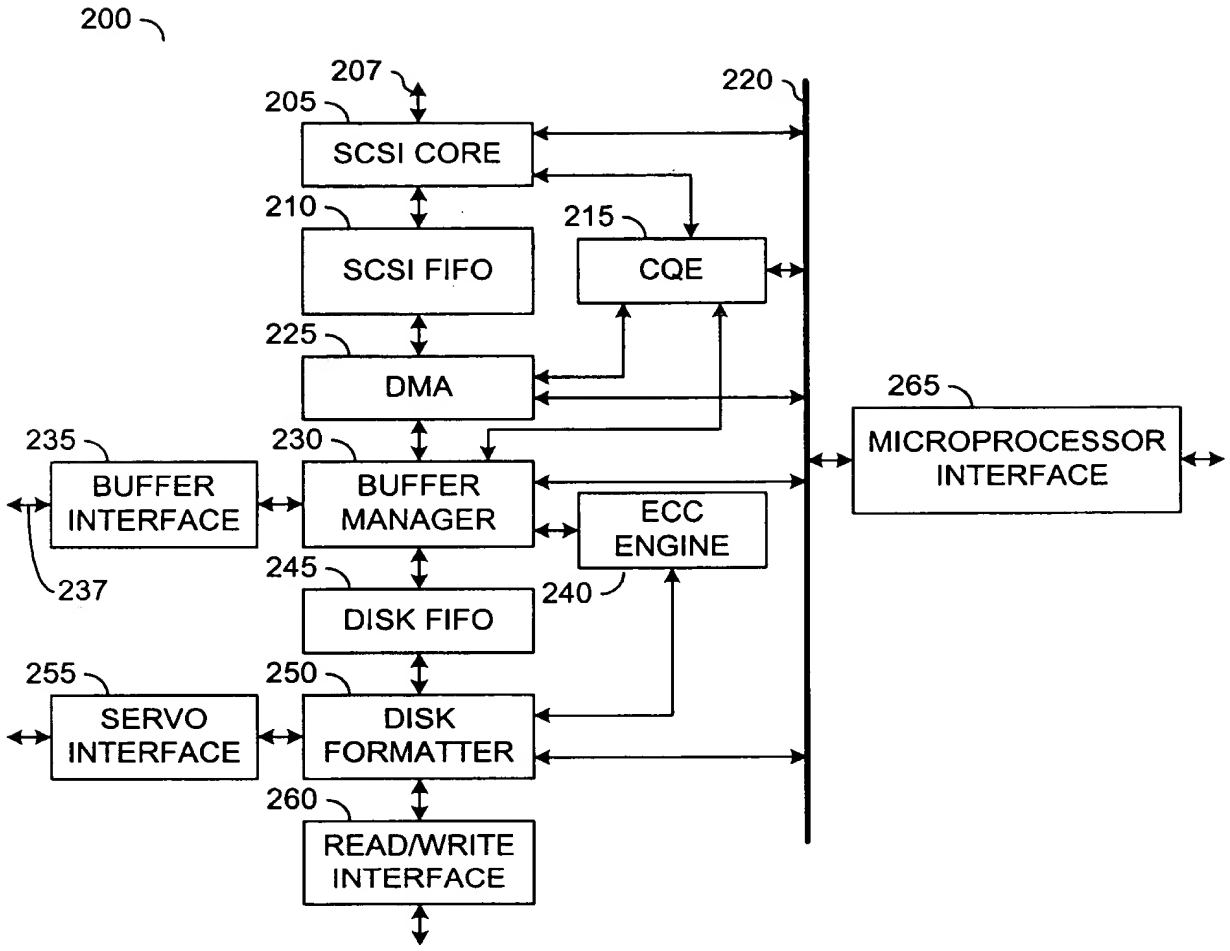

200
207
205
SCSI CORE
220
210
SCSI FIFO
215
CQE
225
DMA
265
MICROPROCESSOR INTERFACE
235
BUFFER INTERFACE
230
BUFFER MANAGER
ECC ENGINE
237
245
240
DISK FIFO
255
SERVO INTERFACE
250
DISK FORMATTER
260
READ/WRITE INTERFACE

FIG. 2

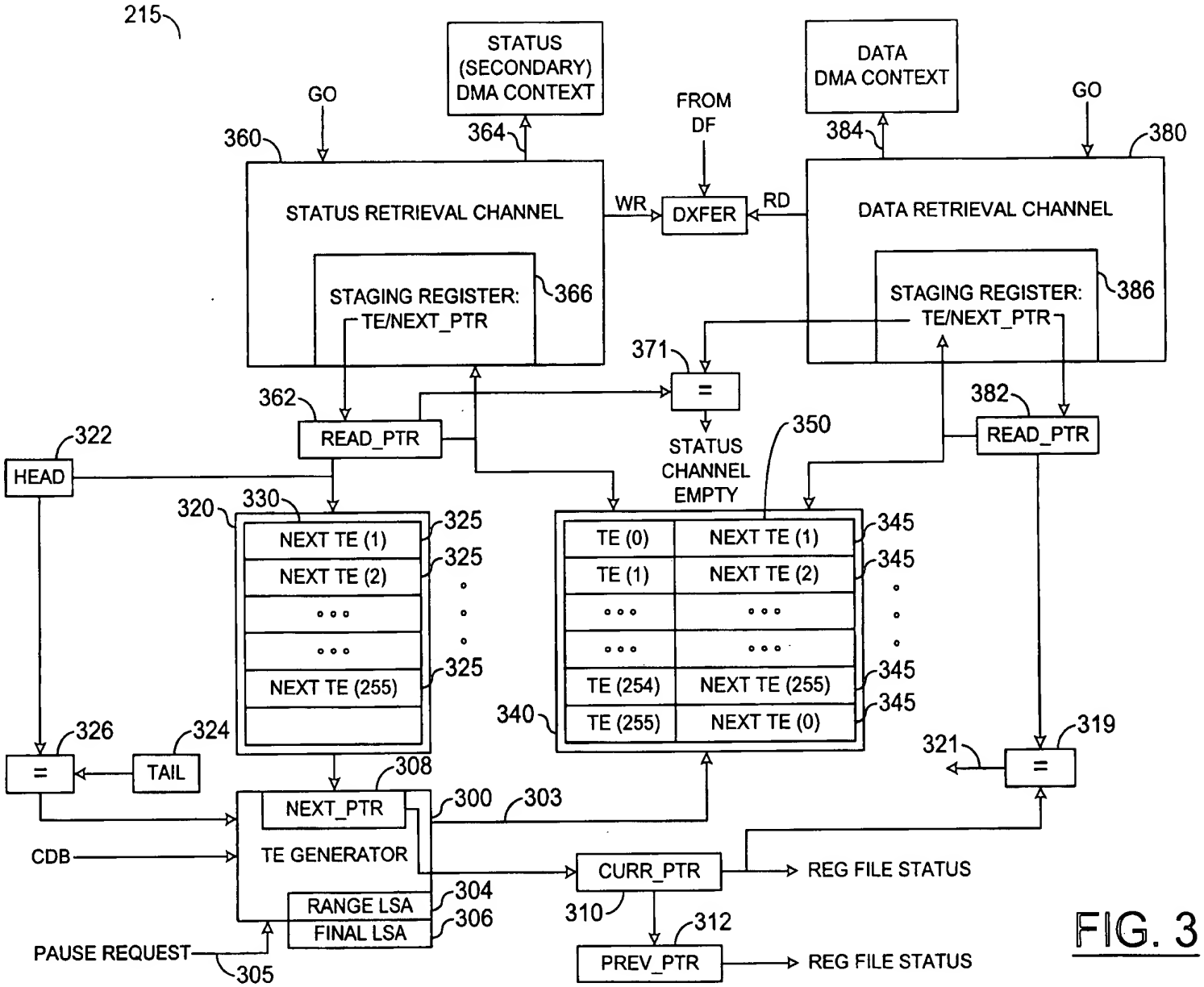

215
STATUS (SECONDARY) DMA CONTEXT
DATA DMA CONTEXT
GO
FROM DF
GO
360
364
384
380
STATUS RETRIEVAL CHANNEL
WR
DXFER
RD
DATA RETRIEVAL CHANNEL
STAGING REGISTER: TE/NEXT_PTR
366
STAGING REGISTER: TE/NEXT_PTR
386
371
=
362
READ_PTR
382
READ_PTR
322
HEAD
STATUS CHANNEL EMPTY
350
320
330
NEXT TE (1)
NEXT TE (2)
NEXT TE (255)
325
TE (0)
NEXT TE (1)
TE (1)
NEXT TE (2)
TE (254)
NEXT TE (255)
TE (255)
NEXT TE (0)
345
340
326
=
324
TAIL
308
NEXT_PTR
300
303
319
321
=
CDB
TE GENERATOR
CURR_PTR
REG FILE STATUS
RANGE LSA
FINAL LSA
304
306
310
312
PREV_PTR
REG FILE STATUS
PAUSE REQUEST
305

FIG. 3

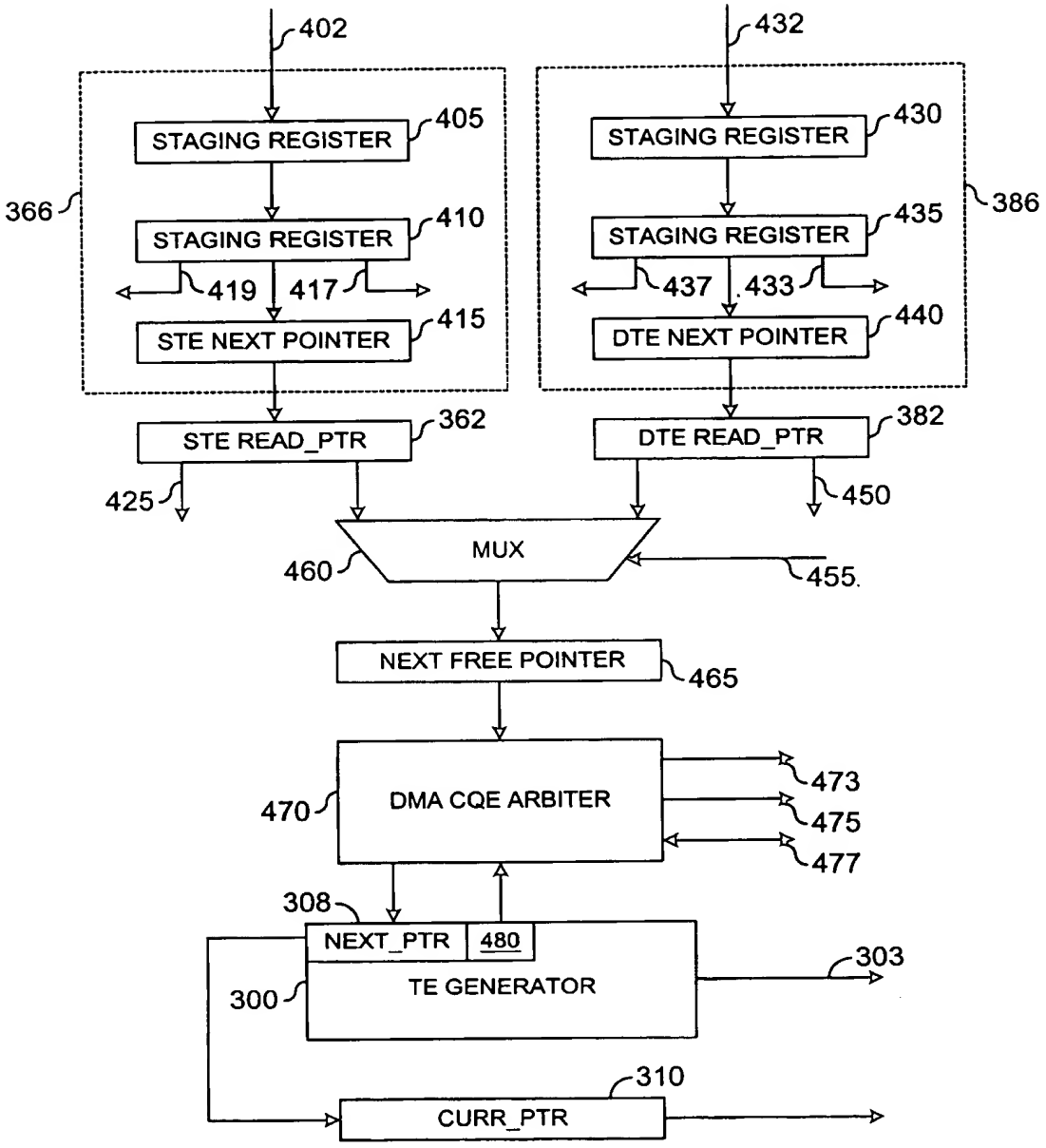

402
432
STAGING REGISTER
405
STAGING REGISTER
430
366
386
STAGING REGISTER
410
STAGING REGISTER
435
419
417
437
433
STE NEXT POINTER
415
DTE NEXT POINTER
440
STE READ_PTR
362
DTE READ_PTR
382
425
450
MUX
460
455
NEXT FREE POINTER
465
DMA CQE ARBITER
470
473
475
477
308
NEXT_PTR
480
TE GENERATOR
303
300
310
CURR_PTR

FIG. 4

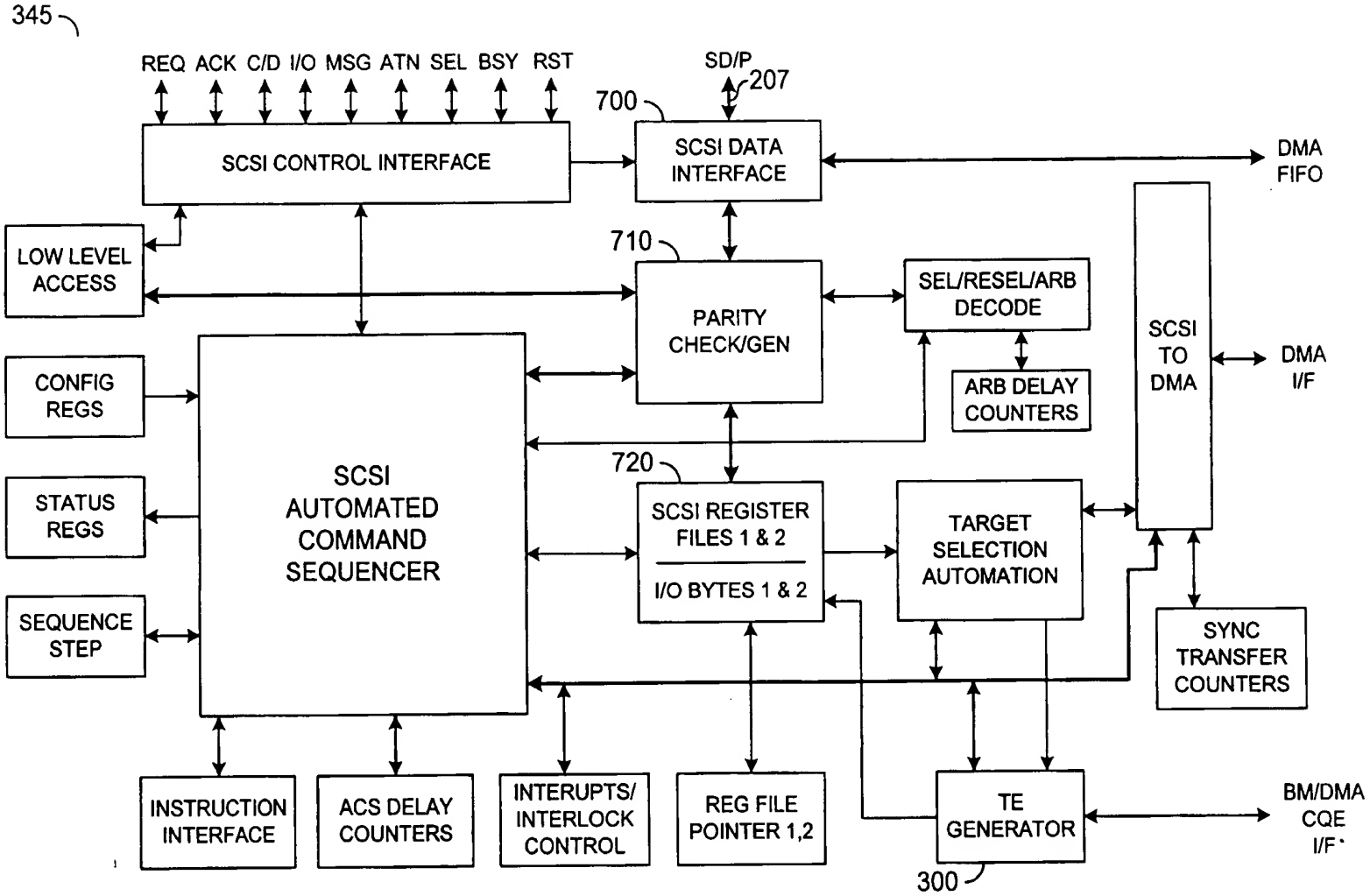
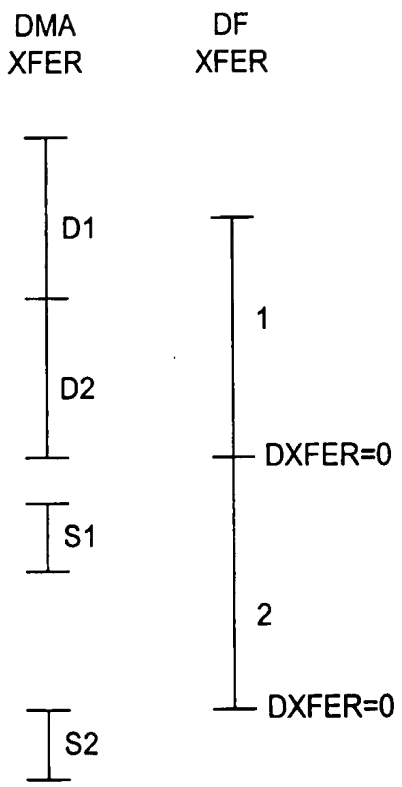
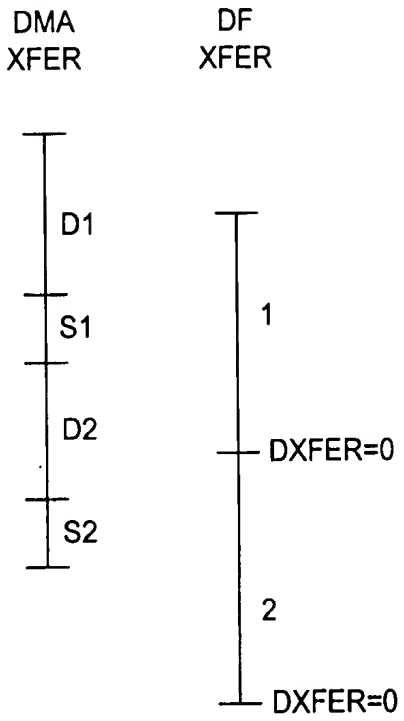

345
REQ ACK C/D I/O MSG ATN SEL BSY RST
SD/P
207
700
SCSI CONTROL INTERFACE
SCSI DATA INTERFACE
DMA FIFO
LOW LEVEL ACCESS
710
PARITY CHECK/GEN
SEL/RESEL/ARB DECODE
ARB DELAY COUNTERS
SCSI TO DMA
DMA I/F
CONFIG REGS
STATUS REGS
SEQUENCE STEP
SCSI AUTOMATED COMMAND SEQUENCER
720
SCSI REGISTER FILES 1 & 2
I/O BYTES 1 & 2
TARGET SELECTION AUTOMATION
SYNC TRANSFER COUNTERS
INSTRUCTION INTERFACE
ACS DELAY COUNTERS
INTERUPTS/ INTERLOCK CONTROL
REG FILE POINTER 1,2
TE GENERATOR
300
BM/DMA CQE I/F

FIG. 5



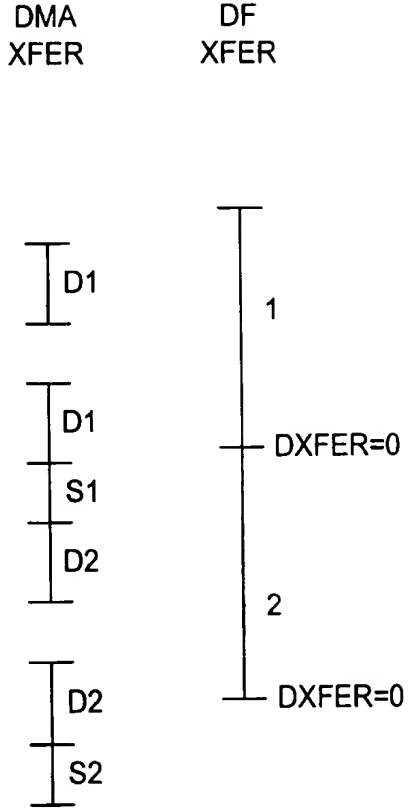
NON-CACHED WRITE

FIG. 6a



CACHED WRITE

FIG. 6b



READ

FIG. 6c

S_SRF1 ADDRESS	S_SRF2 ADDRESS	AUTOMATED COMMANDS		NON-AUTOMATED COMMANDS	
		HIGH BYTE	LOW BYTE	HIGH BYTE	LOW BYTE
0C80h	0CB0h	InitID (3:0)	IDENTIFY	InitID (3:0)	IDENTIFY
0C82h	0CB2h	UNUSED	UNUSED	UNUSED	UNUSED
0C84h	0CB4h	OPCODE	LUN	CDB0 (OPCODE)	CDB1
0C86h	0CB6h	QUEUE CODE	QUEUE TAG	QUEUE CODE	QUEUE TAG
0C88h	0CB8h	LBA (NLSB)	LBA (LSB)	CDB4	CDB5
0C8Ah	0CBAh	LBA (MSB)	LBA (NMSB)	CDB2	CDB3
0C8Ch	0CBCh	SECONDARY LBA (NLSB)	SECONDARY LBA (LSB)	CDB8	CDB9
0C8Eh	0CBEh	SECONDARY LBA (MSB)	SECONDARY LBA (NMSB)	CDB6	CDB7
0C90h	0CC0h	LENGTH (NLSB)	LENGTH (LSB)	CDB12	CDB13
0C92h	0CC2h	LENGTH (MSB)	LENGTH (LMSB)	CDB10	CDB11
0C94h	0CC4h	SRF1S/SRF2S (RO)		SRF1S/SRF2S (RO)	
0C96h	0CC6h	RESERVED BYTE	CONTROL BYTE	CDB14	CDB15
0C98h	0CC8h	SRF1FLL/SRF2FLL		SRF1FLL/SRF2FLL	
0C9Ah	0CCAh	SRF1FLH/SRF2FLH		SRF1FLH/SRF2FLH	
0C9Ch	0CCCh	SRF1TCP/SRF2TCP		SRF1TCP/SRF2TCP	
0C9Eh	0CCEh	SRF1TPP/SRF2TPP		SRF1TPP/SRF2TPP	
0CA0h	0CD0h	SRF1CQES/SRF2CQES		SRF1CQES/SRF2CQES	

FIG. 7a

BYTE	AUTOPOSITIONED	NON AUTOPOSITIONED	REG FILE 1 ADDRESS	REG FILE 2 ADDRESS
BYTE 0	InitID	InitID	0C81h	0CB1h
BYTE 1	IDENTIFY	IDENTIFY	0C80h	0CB0h
BYTE 2	QUEUE CODE	QUEUE CODE	0C87h	0CB7h
BYTE 3	QUEUE TAG	QUEUE TAG	0C86h	0CB6h
BYTE 4	OPCODE	CDB0	0C85h	0CB5h
BYTE 5	LUN	CDB1	0C84h	0CB4h
BYTE 6	LBA (MSB)	CDB2	0C8Bh	0CBBh
BYTE 7	LBA (NMSB)	CDB3	0C8Ah	0CBAh
BYTE 8	LBA (NLSB)	CDB4	0C89h	0CB9h
BYTE 9	LBA (LSB)	CDB5	0C88h	0CB8h
BYTE 10	SLBA (MSB)	CDB6	0C8Fh	0CBFh
BYTE 11	SLBA (NMSB)	CDB7	0C8Eh	0CBEh
BYTE 12	SLBA (NLSB)	CDB8	0C8Dh	0CBDh
BYTE 13	SLBA (LSB)	CDB9	0C8Ch	0CBCh
BYTE 14	LEN (MSB)	CDB10	0C93h	0CC3h
BYTE 15	LEN (NMSB)	CDB11	0C92h	0CC2h
BYTE 16	LEN (NLSB)	CDB12	0C91h	0CC1h
BYTE 17	LEN (LSB)	CDB13	0C90h	0CC0h
BYTE 18	RESERVED BYTE	CDB14	0C97h	0CC7h
BYTE 19	CONTROL BYTE	CDB15	0C96h	0CC6h

FIG. 7b

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			ENSEQ	DISCPRIV	CQETTD	CQELINK	CQEFLAG	CQENACA	CQEREAD	CQEQCODE		CQEInitID			

CQE SEQUENTIAL FIELDS

FIG. 8a

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQEFLLWORD															

CQE FINAL LSA LOW WORD

FIG. 8b

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQEFLHWORD															

CQE FINAL LSA HIGH WORD

FIG. 8c

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			CMDGTMAX	NXTPTRVLD	QFULLBUSY	SEQCMND	RWCMND	AWROK	ACWROK	ACRDOK	TEGIP	CAF	TEFULL	DTEEOFQ	STEEOFQ

CQE STATUS

FIG. 8d

CDB	REGISTERS	REGISTER FILE	TCB 1	TCB 2	TCB 3
LSA=0 LEN=2	FINAL LSA=2 CURRENT POINTER=0 PREVIOUS POINTER=X	PREV. FINAL LSA=X CURRENT POINTER=0 PREVIOUS POINTER=X	FIRST TE=0 LAST TE=X FIRST LSA=0 FINAL LSA=X		
LSA=2 LEN=3	FINAL LSA=5 CURRENT POINTER=1 PREVIOUS POINTER=0	PREV. FINAL LSA=2 CURRENT POINTER=1 PREVIOUS POINTER=0	FIRST TE=0 LAST TE=X FIRST LSA=0 FINAL LSA=X		
LSA=1000 LEN=1	FINAL LSA=1001 CURRENT POINTER=2 PREVIOUS POINTER=1	PREV. FINAL LSA=5 CURRENT POINTER=2 PREVIOUS POINTER=1	FIRST TE=0 LAST TE=1 FIRST LSA=0 FINAL LSA=5	FIRST TE=2 LAST TE=X FIRST LSA=1000 FINAL LSA=X	
LSA=5 LEN=1	FINAL LSA=6 CURRENT POINTER=3 PREVIOUS POINTER=2	PREV. FINAL LSA=1001 CURRENT POINTER=3 PREVIOUS POINTER=2	FIRST TE=0 LAST TE=1 FIRST LSA=0 FINAL LSA=5	FIRST TE=2 LAST TE=2 FIRST LSA=1000 FINAL LSA=1001	FIRST TE=3 LAST TE=X FIRST LSA=5 FINAL LSA=X

FIG. 9

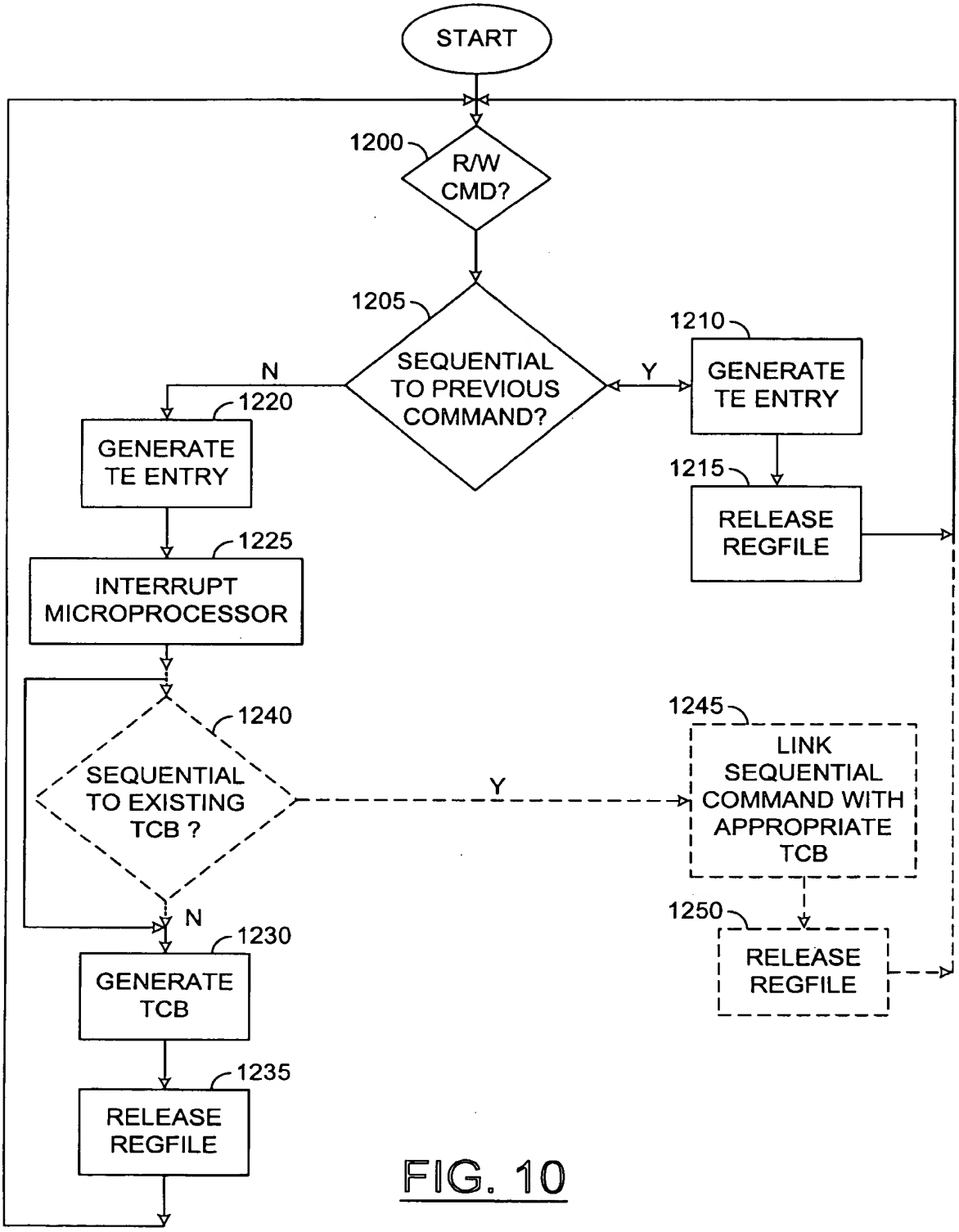

START
1200
R/W CMD?
1205
SEQUENTIAL TO PREVIOUS COMMAND?
N
Y
1210
GENERATE TE ENTRY
1215
RELEASE REGFILE
1220
GENERATE TE ENTRY
1225
INTERRUPT MICROPROCESSOR
1240
SEQUENTIAL TO EXISTING TCB ?
Y
1245
LINK SEQUENTIAL COMMAND WITH APPROPRIATE TCB
1250
RELEASE REGFILE
N
1230
GENERATE TCB
1235
RELEASE REGFILE

FIG. 10